

KA7630/KA7631

Fixed Multi-Output Regulator

Features

- Output Currents up to 0.5A (Output1 & 2)
- Output Current up to 1A with External Transistor (Output3)
- Fixed Precision Output 1 Voltage $5.1V \pm 2\%$
- Fixed Precision Output 2 Voltage $8V \pm 2\%$ (KA7630)
- Fixed Precision Output 2 Voltage $9V \pm 2\%$ (KA7631)
- Control Signal Generator for Output 3 Voltage ($12V \pm 2\%$)
- Reset Facility for Output Voltage1
- Output 2,3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shut Down

Description

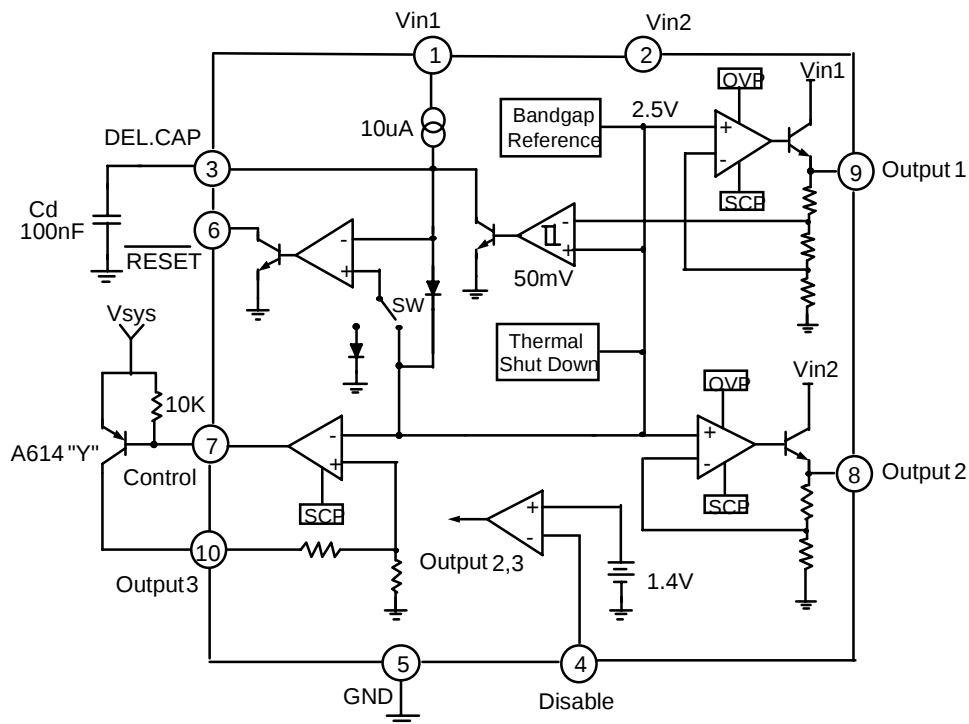
The KA7630/KA7631 is a multi-output positive voltage regulator designed to provide fixed precision output voltages of 5.1V, 8V (7630) / 9V(7631) at current up to 0.5A and 12V at current up to 1A with external PNP transistor.

An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated value. Output2 & 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shutdown.

10-SIP H/S



Internal Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Remark
DC Input Voltage	V _{in}	20	V	-
Disable Input Voltage	V _c	20	V	-
Output Current	I _o	0.5	A	-
Power Dissipation	P _d	1.5	W	No Heatsink
Junction Temperature	T _j	+150	°C	-
Operating Temperature	T _{opr}	0 ~ +125	°C	-

Electrical Characteristics(KA7630)

(Refer to test circuit V_{in1}=7.5V ,V_{in2}=10.5V ,T_j = +25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage 1	V _{o1}	I _{o1} = 10mA 7.5V < V _{in1} < 14V 5mA < I _{o1} < 500mA	5 4.9	5.1 5.1	5.2 5.3	V
Output Voltage 2	V _{o2}	I _{o2} = 10mA 10.5V < V _{in2} < 18V 5mA < I _{o2} < 500mA	7.84 7.7	8 8	8.16 8.3	V
Dropout Output Voltage 1,2	V _{d1,2}	I _{o1,2} = 500mA	-	-	2.5	V
Line Regulation 1,2	ΔV _{o 1,2}	7.5V < V _{in1} < 14V 10.5V < V _{in2} < 18V I _{o1,2} = 200mA	-	-	50 80	mV
Load Regulation 1,2	ΔV _{o 1,2}	5mA < I _{o1} < 500mA 5mA < I _{o2} < 500mA	-	-	100 160	mV
Output Voltage 3	V _{o3}	V _{sys} =13V, I _{o3} =100mA	11.7	12	12.3	V
Line Regulation 3	ΔV _{o3}	13V < V _{in2} < 18V, I _{o3} = 100mA	-	-	120	mV
Load Regulation 3	ΔV _{o3}	5mA < I _{o3} < 1A	-	-	250	mV
Reset Pulse Delay	Trd	C _d = 100nF, Note1	-	25	-	ms
Saturation Voltage in Reset Condition	V _{rL}	I ₆ = 5mA	-	-	0.4	V
Leakage Current at Pin 6	I _{rH}	V ₆ = 10V	-	-	10	μA
Output Voltage Thermal Drift	ST _t	0°C < T _j < +125°C , Note2	-	100		ppm/°C
Short Circuit Output Current	I _{sc1,2}	V _{in1} = 7.5V ,V _{in2} = 10.5V	-	-	1.6	A
Disable Voltage High	V _{disH}	Output 2 Active	0.8	-	2.0	V
Disable Voltage Low	V _{disL}	Output 2 Disabled	0.8	-	2.0	V
Disable Bias Current	I _{dis}	0V < V _{dis} < 7V	-100	-	2	μA
Junction Temperature for TSD	T _{tsd}	Note 2	-	145	-	°C
Quiescent Current	I _q	I _{o1} = 10mA, Output2 Disabled	-	-	2	mA
Reset Threshold Voltage	V _r	K = V _{o1}	K-0.4	K-0.25	K -0.1	V
Reset Threshold Hysteresis	V _{rth}	Note1	20	50	100	mA

Notes:

1. To check the reset circuit ,the reset output is low to discharge the delay capacitor(=C_d). it's less than V_{o1}-0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source(10μA) if it's more than V_{o1}- 0.2V. The equation of delay time is same as below. Trd = (C_d × 2.5) / 10μA
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics(KA7631) (Continued)(Refer to test circuit $V_{in1}=7.5V$, $V_{in2}=11.5V$, $T_j = +25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage 1	V_{o1}	$I_{o1} = 10mA$ $7.5V < V_{in1} < 14V$ $5mA < I_{o1} < 500mA$	5 4.9	5.1 5.1	5.2 5.3	V
Output Voltage 2	V_{o2}	$I_{o2} = 10mA$ $11.5V < V_{in2} < 18V$ $5mA < I_{o2} < 500mA$	8.82 8.65	9 9	9.18 9.35	V
Dropout Output Voltage 1,2	$V_{d1,2}$	$I_{o1,2} = 500mA$	-	-	2.5	V
Line Regulation 1,2	$\Delta V_{o1,2}$	$7.5V < V_{in1} < 14V$ $11.5V < V_{in2} < 18V$ $I_{o1,2} = 200mA$	-	-	50 80	mV
Load Regulation 1,2	$\Delta V_{o1,2}$	$5mA < I_{o1} < 500mA$ $5mA < I_{o2} < 500mA$	-	-	100 160	mV
Output Voltage 3	V_{o3}	$V_{sys} = 13V$, $I_{o3} = 100mA$	11.7	12	12.3	V
Line Regulation 3	ΔV_{o3}	$13V < V_{in2} < 18V$, $I_{o3} = 100mA$	-	-	120	mV
Load Regulation 3	ΔV_{o3}	$5mA < I_{o3} < 1A$	-	-	250	mV
Reset Pulse Delay	Trd	$C_d = 100nF$, Note1	-	25	-	ms
Saturation Voltage in Reset Condition	V_{rL}	$I_6 = 5mA$	-	-	0.4	V
Leakage Current at Pin 6	I_{rH}	$V_6 = 10V$	-	-	10	μA
Output Voltage Thermal Drift	STt	$0^{\circ}C < T_j < +125^{\circ}C$, Note2	-	100	-	ppm/ $^{\circ}C$
Short Circuit Output Current	$I_{sc1,2}$	$V_{in1} = 7.5V$, $V_{in2} = 11.5V$	-	-	1.6	A
Disable Voltage High	V_{disH}	Output 2 Active	0.8	-	2.0	V
Disable Voltage Low	V_{disL}	Output 2 Disabled	0.8	-	2.0	V
Disable Bias Current	I_{dis}	$0V < V_{dis} < 7V$	-100	-	2	μA
Junction Temperature for TSD	T_{tsd}	Note2	-	145	-	$^{\circ}C$
Quiescent Current	I_q	$I_{o1}=10mA$, Output2 Disabled	-	-	2	mA
Reset Threshold Voltage	V_r	$K = V_{o1}$	K-0.4	K-0.25	K -0.1	V
Reset Threshold Hysteresis	V_{rth}	Note1	20	50	100	mA

Notes:

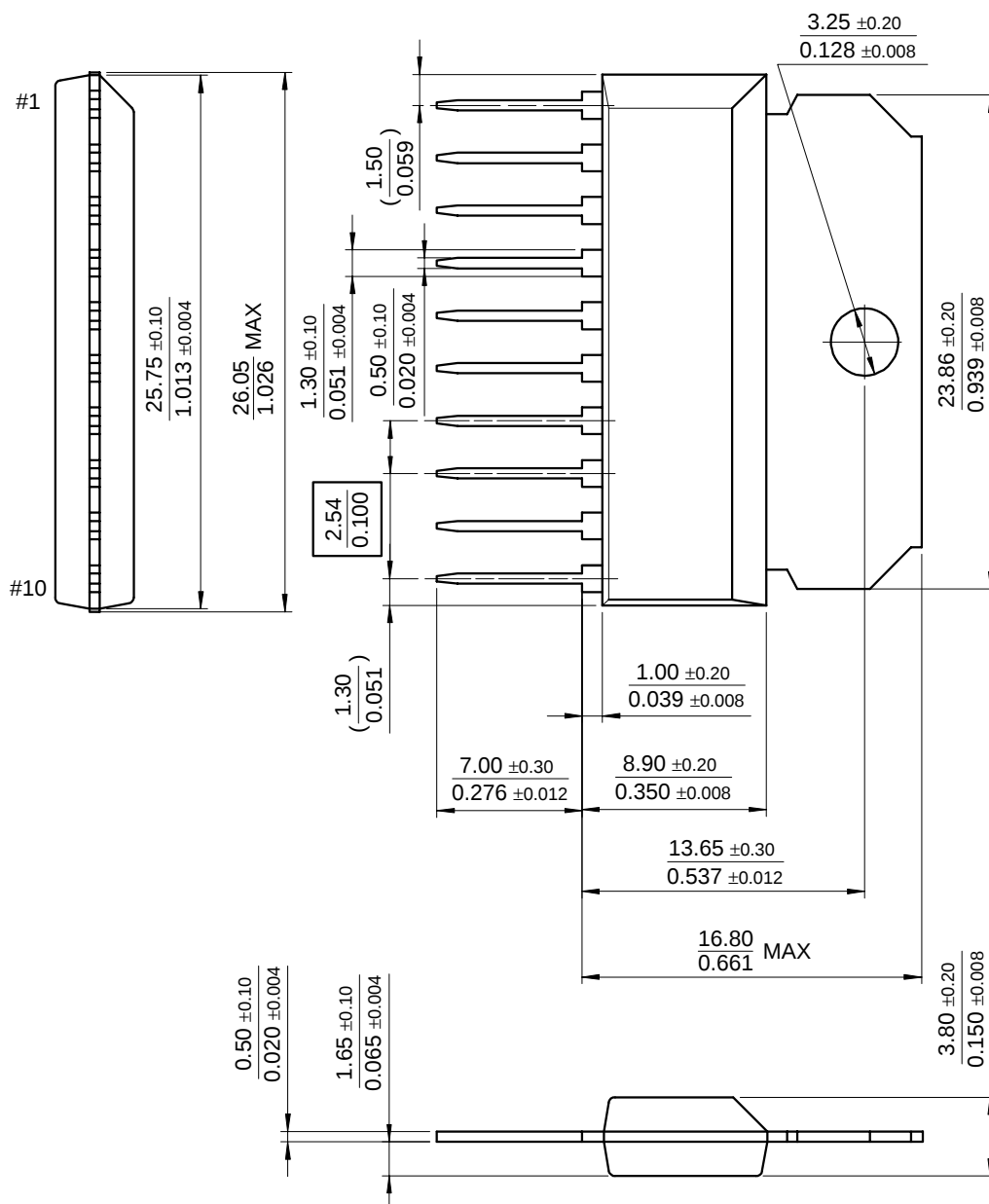
1. To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd). if it's less than $V_{o1}-0.25V$. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source($10\mu A$) if it's more than $V_{o1}-0.2V$. The equation of delay time is same as below. $Trd = (C_d \times 2.5) / 10\mu A$
2. These parameters, although guaranteed, are not 100% tested in production.

Mechanical Dimensions

Package

Dimensions in millimeters

10-SIP-H/S



Ordering Information

Product Number	Package	Operating Temperature
KA7630	10-SIP-H/S	0°C to +125°C
KA7631		

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